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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,822	02/11/2004	Takashi Tagami	NSG-229US	3383

23122 7590 11/09/2004

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EXAMINER	
NGUYEN, JOSEPH H	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,822	TAGAMI ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/762,520.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1A and 1B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Kusuda et al (EP 0335553 A2) or Kusuda et al (JP 2-263668).

With respect to Kusuda et al (EP 0335553 A2).

Regarding claim 1, Kusuda et al discloses on figure 10 an end face light emitting thyristor for emitting light from an end face thereof, comprising a first semiconductor

layer 24 of a first conductivity type, a second semiconductor layer 23 of a second conductivity type, a third semiconductor layer 22 f the first conductivity type, and a fourth semiconductor layer 21 of the second conductivity type stacked in that order on a substrate 1 of the first conductivity type, an electrode 40 provided in such a manner that a part thereof makes ohmic contact with the fourth semiconductor layer in the vicinity of the end face for injecting current into the semiconductor layers, and an insulating layer 30 provided between the fourth semiconductor layer and the part of the electrode that is not made ohmic contact with the fourth semiconductor layer.

Regarding claim 2, Kusuda et al discloses on figure 10 an opening is formed in the part of the insulating layer faced to the end face, the electrode making ohmic contact with the fourth semiconductor layer.

Regarding claim 3, Kusuda et al discloses on figure 9 a self scanning light emitting array comprising a structure in which a plurality of light emitting elements T each having a control electrode G for controlling threshold voltage or current for light emitting operation are arranged, the control electrodes of the light emitting elements are connected to the control electrode of at least one light emitting element located in the vicinity thereof via an interactive resistor R, and a plurality of wiring to which voltage or current is applied are connected to electrodes for controlling the light emission of light emitting elements, and wherein the light element is an end face light emitting thyrsitor as set forth in claim 1 or 2.

Regarding claim 4, Kusuda et al discloses on figure 36 a self scanning light emitting array comprising a structure in which a plurality of light emitting elements T

each having a control electrode G for controlling threshold voltage or current for light emitting operation are arranged, the control electrodes for the light emitting elements are connected to the control electrodes of at least one light emitting element located in the vicinity thereof via an electrically unidirectional element D, and a plurality of wiring to which voltage or current is applied are connected to electrodes for controlling the light emission of light emitting elements, and wherein the light emitting element is an enface light emitting thyristor as set forth in claim 1 or 2.

Regarding claim 5, Kusuda et al discloses on figure 36 the electrically unidirectional element is a diode.

Regarding claim 6, Kusuda et al discloses on figure 36 a self scanning light emitting element array comprising a self scanning transfer element array having such a structure that a plurality of transfer elements D having a control electrode G for controlling threshold voltage or current for transfer operation are arranged, the control electrodes of the transfer elements are connected to the control electrode of at least one transfer element located in the vicinity thereof via an interactive resistor R, power supply lines are connected to the transfer elements by electrical means, and clock lines are connected to the transfer elements, and a light emitting array T having such a structure that a plurality of light emitting elements each having a control electrode for controlling threshold voltage or current are arranged, the control electrodes of the light emitting element array are connected to the control electrodes of said transfer elements by electrical means, and lines for applying current for light emission of the light emitting

element are provided, wherein the light emitting element is an end face light emitting thyristor as set forth in claim 1 or 2.

Regarding claim 7, Kusuda et al discloses on figure 36 a self scanning light emitting array comprising a self scanning transfer element array having such a structure that a plurality of transfer elements each having a control electrode for controlling threshold voltage or current for transfer operation are arranged, the control electrodes of the transfer elements are connected to the control electrode of at least one transfer element located in the vicinity thereof via an electrically unidirectional element D, power supply lines are connected to the transfer elements by electrical means, and clock lines are connected to the transfer elements, and a light emitting element array T having such a structure that a plurality of light emitting elements each having a control electrode for controlling threshold voltage or current are arranged, the control electrodes of the light emitting element array are connected to the control electrodes of said transfer elements by electrical means, and lines for applying current for light emission of the light emitting element are provided, wherein the light emitting element is an end face light emitting thyrsitor as set forth in claim 1 or 2.

Regarding claim 8, Kusuda et al discloses on figure 36 the electrically unidirectional element D is a diode.

With respect to Kusuda et al (JP 2-263668).

Regarding claims 1-8, Kusuda et al discloses on figures 6-7 all the structures set forth in the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

JN
November 12, 2004.

JEROME JACKSON
PRIMARY EXAMINER